**CMPEN 270: Digital Design: Theory and Practice**

**Module 4 Lab: From Logic to Gates**

**Due: 2/6/22**

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**Grading Rubric**

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| **Criteria** | **Grade** |
| Initial grade, based on how well the functional specification is met  Excellent (exceptional achievement) 90-100%  Good (extensive achievement) 80-89%  Satisfactory (acceptable achievement) 72-79%  Poor (minimal achievement) 65 to 71%  Failure (inadequate achievement) 0-64% | / 25 |
| Modification for design documents  Block diagrams  State diagrams  State tables  Other |  |
| Modification for coding style, comments, efficiency  Header comments for files  Other comments (informative but not excessive)  Proper code indenting, alignment, use of whitespace  Code is clean (doesn't have commented out code without a good reason)  Self documenting code (good signal and component names, clear structure, etc.)  General approach (algorithms)  Coding details (operations)  Proper use of components  VHDL matches design documents  Other |  |
| Modification for sections in this report  Design  Verification  Evaluation  Questions  Other |  |
| Bonus (optional challenge, etc.) |  |
| Penalties  No grade until all deliverables are submitted, late submission penalty for anything submitted late  Late submission: (<1 day) -10%, (<1 week) -30%, (<2 weeks) -50%, (>=2 weeks) -99%  Attachments missing, not in order, instructions not followed: -10%  Other |  |
| TOTAL (Max is 100% of total points unless specified otherwise in handout) | / 25 |

**ACKNOWLEDGEMENT**

This work is entirely my own and I did not provide any assistance except as noted.

100% Robert Myers \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Robert Myers\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**ATTACHMENTS**

The following are attached, in this order:

* Starting Circuit worksheet
* 7-Segment Digit Design Worksheet
* 7-Segment Digit Verification Worksheet

**DESIGN**

See 7-Segment Digit Design Worksheet.

**VERIFICATION**

I’ll start by answering the questions in the Lab04 Handout:

**-Are the Verification Worksheet and the Design Worksheet identical?**

Yes, the two are identical.

**-Does it meet the functional specification at the beginning of the module?**  
Yes, the first three digits are turned off and the right-most digit is turned on and displaying the correct corresponding letter in hexadecimal.

To test and verify my solution was correct, I programmed my FPGA with my attempted code. I started by turning on SW0, observed the right-most LED change to a 1 (B and C on) and then went back to my .vhl file to review the sum-of-products was correct. Once this was verified, I repeated the process for the remaining combinations of SW0, SW1, SW2, SW3.

**EVALUATION**

No performance metrics are required for this lab.

**QUESTIONS**

There are no questions for this lab.